ABSTRACT

A scan test circuit includes a scan flip-flop that receives a reset signal, a data signal, a scan data signal, and a scan shift enable signal selecting either the data signal or the scan data signal. A reset control circuit controls the reset signal according to the scan shift enable signal. Even if the reset signal originates in a combinatorial circuit, the reset control circuit can prevent the flip-flop from being reset during a scan shift sequence, without the need for external control of the reset signal. Further control of the reset signal can be provided by a mask circuit. These reset control features enable improved fault coverage to be obtained with a reduced number of external input terminals, a reduced number of test patterns, and only a small amount of additional test circuitry.